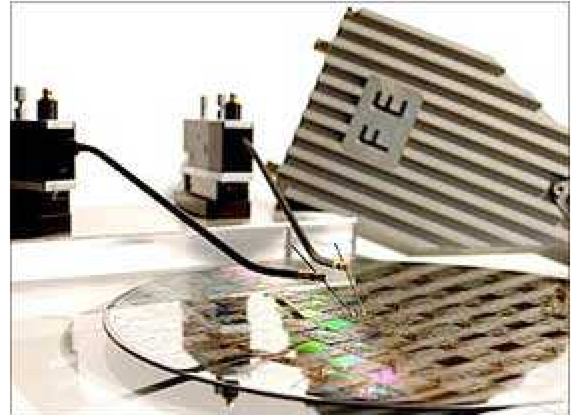
aixACCT
advanced customized characterization technologies

FeRAM Cell Tester

Ferroelectric Random Access Memory Cell Tester

Memory window information based on analog hysteresis measurements on single cell capacitors after full integration process



Field of application

Production of FeRAM

- Quality control during production based on memory window information which is not influenced by deviation of CMOS process
- Single shot hysteresis data at MHz operation speed
- Classification of bit failure instead of bit failure identification

Highlights/Benefits

- Feedback for process optimization during production
- Time efficient testing in the MHz range
- Applicable to 2T-2C cell design and 1T-1C cell design
- Memory window information from analog test data
- Customized adaptation to available test environment
- Update service
- User support

Program features

Hysteresis, PUND tests and other test procedures can be run on a single cell.

Rise times down to 1 µs are available. Self designed pulse trains can be used to test various kinds of failure mechanisms. Pre-polarization pulse parameters can be set independently from the test sequence.

Test sequences with the same pulse train with varying amplitude at constant pulse width or with constant amplitude at varying pulse width can be performed using the Access Time software.

These tests are based on the patented In-situ compensation of the parasitic capacitance.

- Free update service for 18 months
- Individual updates
- Maintenance service

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FeRAM Cell Tester

User support

We provide comprehensive and prompt support to our customers:

- Complete printed documentation, hotline help, on-site implementation
- Free technical support for 100 days
- Low cost annual maintenance service

Features

The FeRAM Cell Tester controls the BL, WL, PL of a full memory cell to record the hysteresis loop of a fully integrated memory cell. The FeRAM Cell Tester generates the required timing.

If the chip offers a layout change, the automatic acquisition of the material properties on a larger array can be done. In this case the FeRAM Cell Tester operates in conjuntion with a switch box system and a probing station. The software of the FeRAM Cell Tester automatically adjusts parameter sets such as those for in-situ compensation etc.

Statistical evaluation is offered by the aixPlorer. E.g. the memory window of a single bit as well as the memroy window distribution on a die or wafer can be derived. But any acquired parameter can be investigated with respect to statistics.

The major benefit of the FeRAM Cell Tester is the important information for process optimization in order to improve yield and therefore to reduce cost as well as reduce the time to market. The correlation of results of the digital and the analog tests offers essential new knowledge.

Specifications

The FeRAM Cell Tester comprises all functionality of high resolution measurements and speed down to the microsecond region.

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